1. GENERAL DESCRIPTION

The EM78451 is an 8-bit microprocessor designed and developed with low-power and high speed CMOS technology. Its operation kernel is implemented with RISC-like architecture. and is available in the mask ROM version. This device is equipped with the Serial Peripheral Interface (SPI) function and an easy-implemented RS-232. The EM78451 is very suitable for the wired communication. Only 58 easy-to-learn instructions are needed and the user's program can be emulated with EMC In-Circuit Emulator (ICE).

2. FEATURES

- Operating voltage range: 2.3V~5.5V.
- Operating temperature range: 0°C~70°C.
- Operating frequency rang (base on2 clocks):
  * Crystal mode: DC~20MHz at 5V, DC~8MHz at 3V, DC~4MHz at 2.3V.
  * RC mode: DC~4MHz at 5V, DC~4MHz at 3V, DC~4MHz at 2.3V.
- Low power consumption:
  * Less then 3 mA at 5V/4MHz
  * Typically 10 μA during sleep mode
- Serial Peripheral Interface (SPI) available.
- 4K × 13 bits on chip ROM (EM78451).
- 11 special function registers.
- 140× 8 bits on chip general-purposed registers.
- 5 bi-directional I/O ports (35 I/O pins).
- 3 LED direct sinking pins with internal serial resistors.
- Built-in RC oscillator with external serial resistor, ±10% variation.
- Built-in power-on reset.
- Five stacks for subroutine nesting.
- 8-bit real time clock/counter (TCC) with overflow interrupt.
- Two machine clocks or four machine clocks per instruction cycle.
- Power down mode.
- Programmable wake up from sleep circuit on I/O ports.
- Programmable free running on-chip watchdog timer.
- 12 wake-up pins.
- 2 open-drain pins.
- 2 R-option pins.
- 32 programmable pull-high input pins.
- Package types:
  * 40 pin DIP 600mil : EM78451AP.
  * 44 pin QFP : EM78451AQ.

- Four types of interrupts.
  * External interrupt (/INT).
  * SPI transmission completed interrupt.
  * TCC overflow interrupt.
  * Timer1 comparator match interrupt.

3. PIN ASSIGNMENT

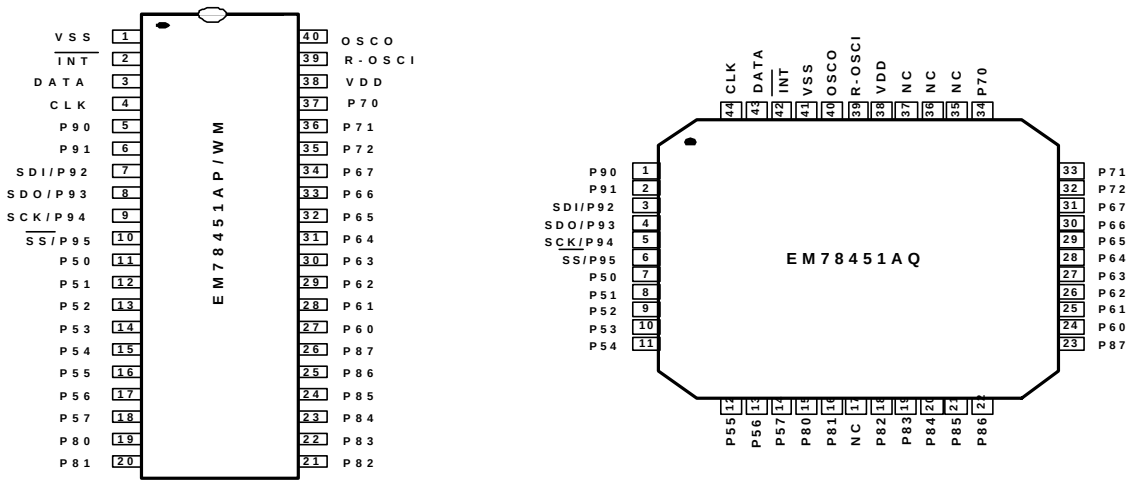


Fig. 1 Pin assignment

Table 1 Pin description

Symbol	Pin No.	Type	Function Description
R-OSCI	39	I	* In XTAL mode: Crystal input; In internal C, external R mode: 56K ohm±5% pull high for 1.8432MHz.
OSCO	40	O	* In XTAL mode: Crystal output; In RC mode: Instruction clock output.
P90~P95	5~10	I/O	* General bi-directional I/O port. All of its pins can be pulled-high by software. * P90 and P91 are pin-change wake up pins.
P80~P87	19~26	I/O	* General bi-directional I/O port. All of its pins can be pulled-high by software. * P80 and P81 are also used as the R-option pins.
P70~P72	37~35	I/O	* LED direct-driving pin with internal serial resistor is used as output and is software defined.
CLK	4	I/O	* By connecting P74 and P76 together. * P74 can be pulled-high by software and it is also a pin-change wake up pin. * P76 can be defined as an open-drain output.
DATA	3	I/O	* By connecting P75 and P77 together. * P75 can be pulled-high by software and it is also a pin-change wake up pin. * P77 can be defined as an open-drain output.
P60~P67	27~34	I/O	* General bi-directional port. All of its pins can be pulled-high by software, and pin-change wake up pins.
P50~P57	11~18	I/O	* General bi-directional I/O port. All of its pins can be pulled-high * *

			Individually by software.
VDD	38	-	* Power supply pin.
VSS	1	-	* Ground pin.
/INT	2	I	* An interrupt schmitt-triggered pin. The function of interrupt triggers at the falling edge. Users can enable it by software. The internal pull-up resistor is around 50K ohm.
SDI	7	I/O	* Serial data in for SPI
SDO	8	I/O	* Serial data out for SPI.
SCK	9	I/O	* Serial clock for SPI.
/SS	10	I/O	* /Slave select for SPI.

4. FUNCTION DESCRIPTION

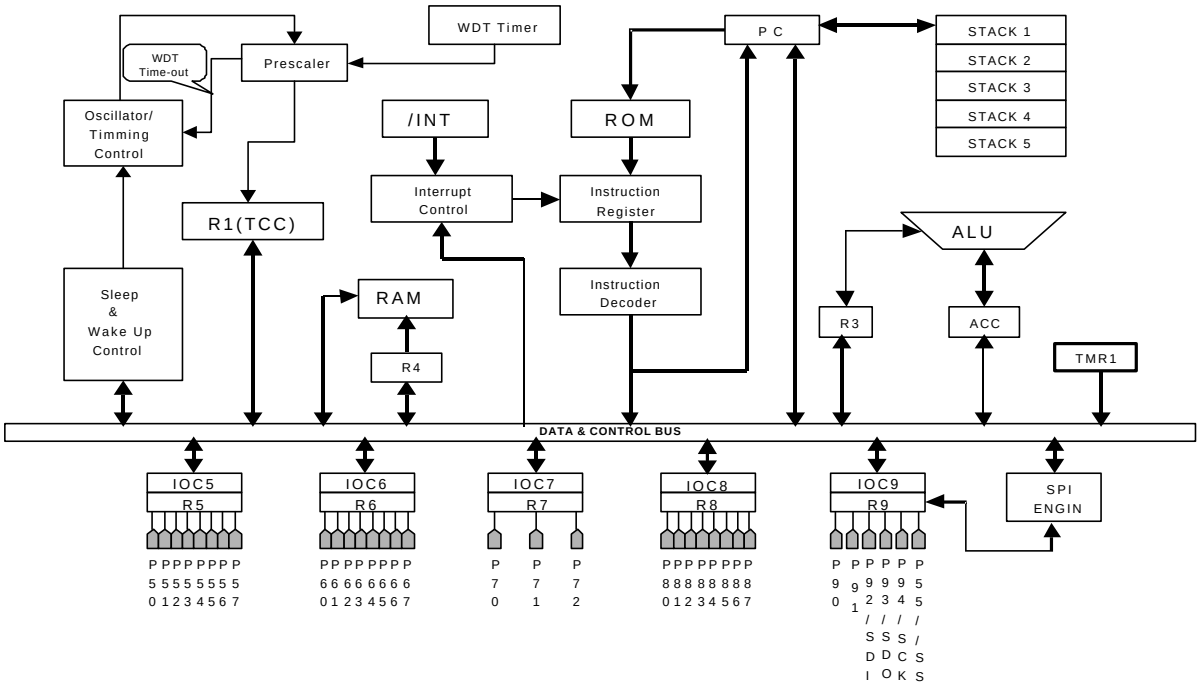


Fig. 2 Functional Block Diagram

4.1 Operational Registers

1. R0 (Indirect Address Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

2. R1 (TCC)

- Increased by the instruction cycle clock.
- Written and read by program as any other register.

3. R2 (Program Counter) & Stack

- R2 and the hardware stacks are 12 bits wide.
- The structure is depicted in Fig. 3.

- Generates 4K × 13 on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- All the R2 bits are set to "1"s as a RESET condition occurs.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows jump to any location on one page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.
- "MOV R2, A" allows the loading of an address from the "A" register to the lower 8 bits of PC, and the ninth and tenth bits (A8~A9) of PC are cleared.
- "ADD R2, A" allows a relative address be added to the current PC, and the ninth and tenth bits of PC are cleared.
- Any instruction that is written to R2 (e.g. "ADD R2, A", "MOV R2, A", "BC R2,6",·····) (except "TBL") will cause the ninth and tenth bits (A8~A9) of PC to be cleared. Thus, the computed jump is limited to the first 256 locations of any program page.
- "TBL" allows a relative address be added to the current PC (R2+A→R2), and contents of the ninth and tenth bits (A8~A9) of PC are not changed. Thus, the computed jump can be on the second (or third, 4th) 256 locations on one program page.
- In case of EM78451, the most significant bit (A10,A11) will be loaded with the content of bit PS0 ~PS1 in the status register (R3) upon the execution of a "JMP", "CALL", or any other instructions which write to R2.
- All instructions are single instruction cycle (fclk/2 or fclk/4) except for the instruction that would change the contents of R2. Such instruction will need one more instruction cycle.

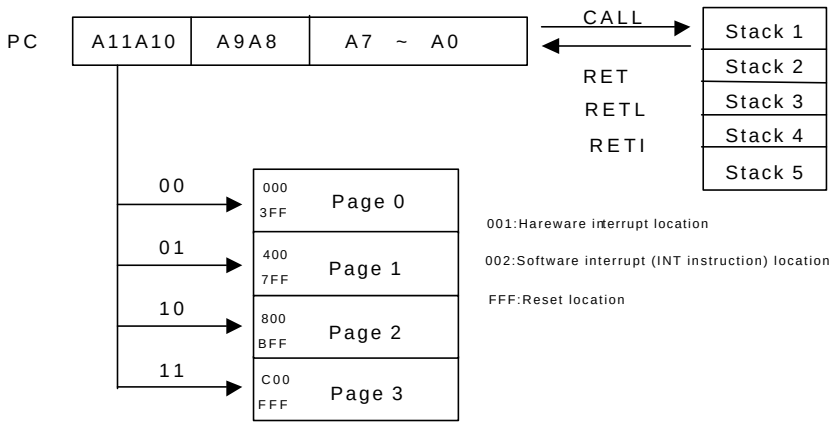


Fig. 3 Program counter organization

4. R3 (Status Register)

7	6	5	4	3	2	1	0
GP	PS1	PS0	T	P	Z	DC	C

- Bit 0 (C) Carry flag
- Bit 1 (DC) Auxiliary carry flag
- Bit 2 (Z) Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.
- Bit 3 (P) Power down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.
- Bit 4 (T) Time-out bit. Set to 1 with the "SLEP" and the "WDTC" commands, or during power up and reset to 0 with WDT timeout.
- Bits 5 (PS0) ~ 6 (PS1) Page select bits. PS0~PS1 are used to pre-select a program memory page. When executing a "JMP", "CALL", or other instructions which causes the program counter to be changed (e.g. MOV R2, A), PS0~PS1 are loaded into the 11th and 12th bits of the program counter where it selects one of the available program memory pages. Note that RET (RETL, RETI) instruction does not change the PS0~PS1 bits. That is, the return will always be to the page from where the subroutine was called, regardless of the current setting of PS0~PS1 bits. PS1 bit is not used (read as "0") and cannot be modified in EM78451.

PS1	PS0	Program memory page [Address]
0	0	Page 0 [000-3FF]
0	1	Page 1 [400-7FF]
1	0	Page 2 [800-BFF]
1	1	Page 3 [C00-FFF]

- Bit 7 (GP) General read/write bit.

5. R4 (RAM Select Register)

- Bits 0~5 are used to select the registers (address: 00~3F) in the indirect addressing mode.
- Bits 6~7 determine which bank is activated among the 4 banks.
- If no indirect addressing is used, the RSR is used as an 8-bit general-purposed read/writer register.
- See the configuration of the data memory in Fig. 4.

6. R5~R8 (Port 5 ~ Port8)

- Four general 8 bits I/O registers
- Both P74 and P76 read or write data from the DATA pin, while both P75 and P77 read or write data from the CLK pin.

7. R9 (Port9)

- A general 6-bit I/O register. The values of the two most significant bits are read as "0".

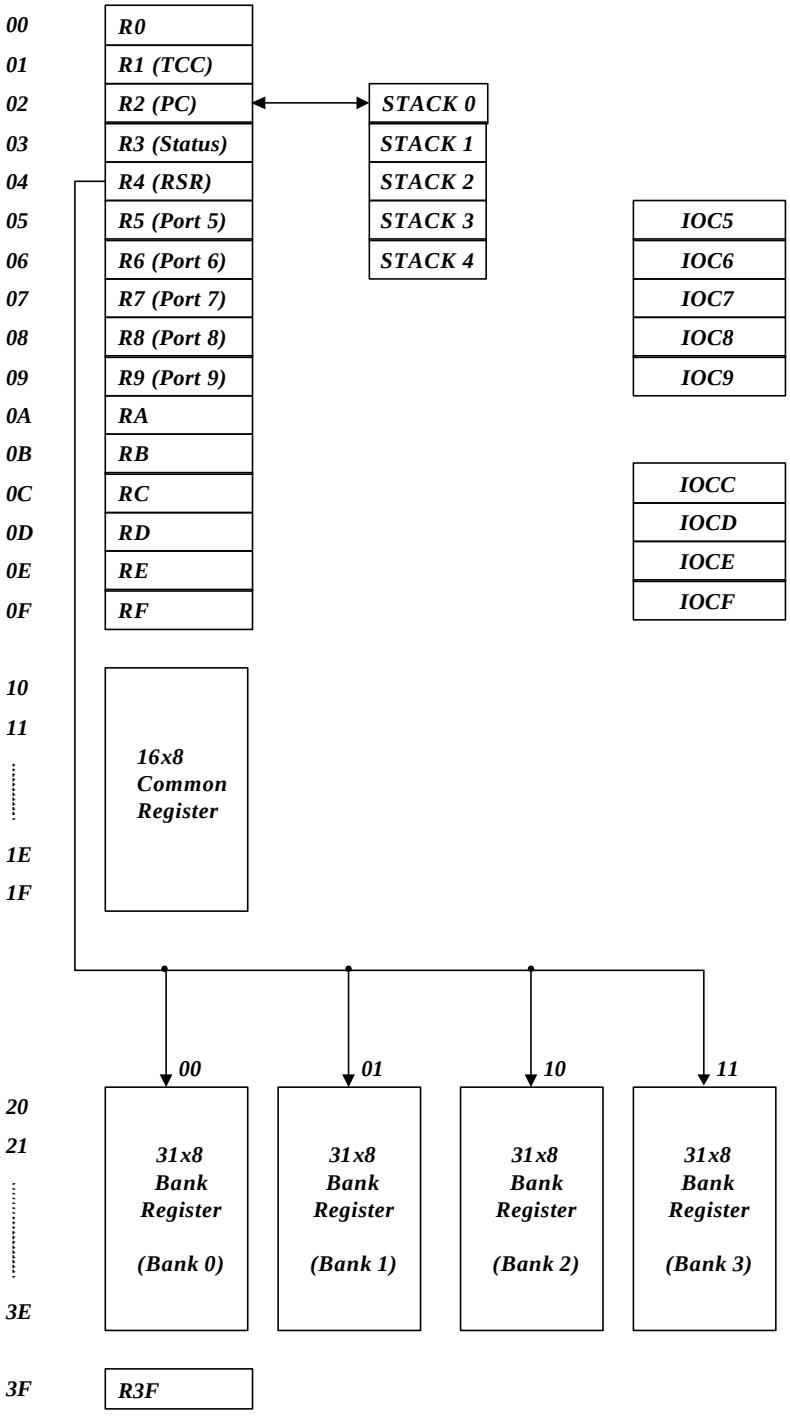


Fig. 4 Data Memory Configuration

8. RA (SPIRB: SPI Read Buffer)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0A	SPIRB/RA	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0

- SRB7~SRB0 are the 8-bit data when transmission is completed through SPI.

9. RB (SPIWB: SPI Write Buffer)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0B	SPIWB/RB	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0

- SWB7~SWB0 are the 8-bit data that wait for transmission through SPI.

10. RC (SPIS: SPI Status Register)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	SPIS/RC	--	--	--	TM1IF	OD3	OD4	RBFIF	RBF

- TM1IF (bit 4):

  1 = In timer1 mode, receiving completed, and an interrupt occurs if enabled.

  0 = In timer1 mode, receiving not completed yet, and an interrupt does not occur.

- OD3 (bit 3):Open Drain Control bit

  1 = Open-Drain enable for SDO,

  0 = Open-Drain disable for SDO.

- OD4 (bit 2):Open-Drain Control bit

  1 = Open-Drain enable for SCK,

  0 = Open-Drain disable for SCK.

- RBFIF (bit 1): Read Buffer Full Interrupt flag

  1 = Receive is finished, SPIRB is fully exchanged, and an interrupt occur if enable.

  0 = Receive is not finish yet; SPIRB is not already fully exchanged.

- RBF (bit 0): Read Buffer Full flag

  1 = Receiving completed; SPIRB is fully exchanged.

  0 = Receiving not completed yet; and SPIRB has not fully exchanged.

11. RD (SPIC: SPI Control Register)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0D	SPIC/RD	CES	SPIE	SRO	SSE	-	SBRS2	SBRS1	SBRS0

- CES (bit 7): Clock Edge Select bit

  1 = Data shifts out on falling edge, and shifts in on rising edge. Data is on hold during the high level.

  0 = Data shifts out on rising edge, and shifts in on falling edge. Data is on hold during the low level.

- SPIE (bit 6): SPI Enable bit

1= Enable SPI mode

0= Disable SPI mode

- SRO (bit 5): SPI Read Overflow bit

  1 = A new data is received while the previous data is still being held in the SPIB register. In this situation, the data in SPIS register will be destroyed. To avoid setting this bit, users had better read SPIRB register even if only the transmission is implemented.

  0 = No overflow.

  <Note>: This can only occur in slave mode.

- SSE (bit 4): SPI Shift Enable bit

  1 = Start to shift, and keep on 1 while the current byte is still being transmitted.

  0 = Reset as soon as the shifting is complete, and the next byte is ready to shift.

  <Note>: This bit will reset to 0 at every one-byte transmission by the hardware

- SBRS (bit 2~bit 0): SPI Baud Rate Select bits

  SPI baud rate table is illustrated in the SPI section of this specification.

12. RE (TMR1: Timer1 register)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0E	TMR1/RE	TMR17	TMR16	TMR15	TMR14	TMR13	TMR12	TMR11	TMR10

- TMR17~TMR10 is bit set of timer1 register and it increases until the value matches PWP and then it resets to 0.

13. RF (PWP: Pulse width preset register)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0F	PWP/RF	PWP7	PWP6	PWP5	PWP4	PWP3	PWP2	PWP1	PWP0

- PWP7~PWP0 is bit set of pulse width preset in advance for the desired baud clock width.

14. R20~R3E (General Purpose Register)

- RA~R1F, and R20~R3E (including Banks 0~3) are general-purpose registers.

15. R3F (Interrupt Status Register)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x3F	ISR/R3F	-	-	-	-	TM1IF	SPIIF	EXIF	TCIF

- Bit 0 (TCIF) TCC timer overflow interrupt flag. Set as TCC overflow; flag cleared by software.
- Bit 1 (EXIF) External interrupt flag. Set by falling edge on /INT pin, flag cleared by software
- Bit 2 (SPIIF) SPI interrupt flag. Set by completion of data transmission, flag cleared by software.
- Bit 3 (TM1IF) Timer1 interrupt flag. Set by the comparator at Timer1 application, flag cleared by software.

- Bits 2~7 are not used and read as "0".
- "1" means interrupt request, "0" means non-interrupt.
- R3F can be cleared by instruction, but cannot be set by instruction.
- IOCF is the interrupt mask register.
- Note that to read R3F will result of "logic AND" of R3F and IOCF.

4.2 Special Purpose Registers

1. A (Accumulator)

- Internal data transfer, or instruction operand holding.
- A non-addressable register.

2. CONT (Control Register)

7	6	5	4	3	2	1	0
/PHEN	/INT	-	-	PAB	PSR2	PSR1	PSR0

- Bit 7 (/PHEN) I/O pin pull-high enable flag.

  0: For P60~P67, P74~P75 and P90~P95, the pull-high function is enabled.

  1: The pull-high function is disabled.
- Bit 6 (INT) An interrupt enable flag cannot be written by the CONTW instruction.

  0: interrupt masked by the DISI instruction.

  1: interrupt enabled by the ENI or RETI instruction.
- Bit4, 5 Not used, and to be read as "0".
- Bit 3 (PAB) Prescaler assignment bit.

  0: TCC

  1: WDT
- Bit 0 (PSR0) ~ Bit 2 (PSR2) TCC/WDT prescaler bits.

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

- Bits 0~3, and 7 of the CONT register are readable and writable.

3. IOC5 ~ IOC9 (I/O Port Control Register)

- "1" put the relative I/O pin into high impedance, while "0" put the relative I/O pin as output.
- Both P74 and P76 should not be defined as output pins at the same time, This also applies to both P75 and P77.
- Only the lower 6 bits of the IOC9 register are used.

4. IOCC (T1CON: Timer1 control register)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	T1CON/IOCC	0	0	0	0	0	TM1E	TM1P1	TM1P0

- TM1E (bit2): Timer1 Function Enable bit

  1 = Enable timer1 function.

  0 = Disable timer1 function as default.
- TM1P (bit1~bit0): Timer1 Prescaler bit

  Timer1 prescaler table for FOSC will be illustrated in the Section on Timer1 in later pages.

5. IOCD (Pull-high Control Register)

7	6	5	4	3	2	1	0
S7	-	-	-	/PU9	/PU8	/PU6	/PU5

- The default values of /PU5, /PU6, /PU8, and /PU9 are one which means the pull-high function is disabled.
- /PU6 and /PU9 are "AND" gating with /PHEN, that is, when each one is written as"0," pull high is enabled.
- S7 defines the driving ability of the P70-P72.

  0: Normal output.

  1: Enhance the driving ability of LED.

6. IOCE (WDT Control Register)

7	6	5	4	3	2	1	0
-	ODE	WDTE	SLPC	ROC	-	-	/WUE

- Bit 0 (/WUE) Control bit used to enable the wake-up function of P60~P67, P74~P75, and P90~P91.

  0: Enable the wake-up function.

  1: Disable the wake-up function.

  The /WUE bit can be read and written.
- Bit 3 (ROC) ROC is used for the R-option. Setting ROC to "1" will enable the status of R-option pins (P80, P81) to be read by the controller. Clearing ROC will disable the R-option function. Otherwise, the R-option function is introduced. Users must connect the P81 pin or/and P80 pin to VSS by a

560KΩ external resistor (Rex). If Rex is connected/disconnected with VDD, the status of P80 (P81) will be read as "0"/"1" (refer to Fig. 7(b)). The ROC bit can be read and written.

- Bit 4 (SLPC) This bit is set by hardware at the falling edge of wake-up signal and is cleared in software. SLPC is used to control the oscillator operation. The oscillator is disabled (oscillator is stopped, and the controller enters the SLEEP2 mode) on the high-to-low transition and is enabled (the controller is awakened from SLEEP2 mode) on low-to-high transition. In order to ensure the stable output of the oscillator, once the oscillator is enabled again, there is a delay for approximately 18 ms (oscillator start-up timer (OST)) before the next program instruction is executed. The OST is always activated by wake-up from sleep mode whether the Code Option bit ENWDT is "0" or not. After waking up, the WDT is enabled if Code Option ENWDT is "1". The block diagram of SLEEP2 mode and wake-up caused by input triggered is depicted in Fig. 5. The SLPC bit can be read and written.
- Bit 5 (WDTE) Control bit used to enable Watchdog timer.

  The WDTE bit can be used only if ENWDT, the CODE Option bit, is "1". If the ENWDT bit is "1", then WDT can be disabled/enabled by the WDTE bit.

  0: Disable WDT.

  1: Enable WDT.

  The WDTE bit is not used if ENWDT, the CODE Option bit ENWDT, is "0". That is, if the ENWDT bit is "0", WDT is always disabled no matter what the WDTE bit is.

  The WDTE bit can be read and written.
- Bit 6 (ODE) Open-drain control bit.

  0: Both P76 and P77 are normally I/O pins.

  1: Both P76 and P77 pins have the open-drain function inside.

  The ODE bit can be read and written.
- Bits 1~2, and 7 Not used.

7. IOCF (Interrupt Mask Register)

7	6	5	4	3	2	1	0
-	-	-	-	TM1IE	SPIIE	EXIE	TCIE

- Bit 0 (TCIE) TCIF interrupt enable bit.

  0: disable TCIF interrupt

  1: enable TCIF interrupt
- Bit 1 (EXIE) EXIF interrupt enable bit.

  0: disable EXIF interrupt

1: enable EXIF interrupt

- Bit 2 (SPIIE) SPI interrupt enable bit.

  0: disable SPI interrupt

  1: enable SPI interrupt

- Bit 3 (TM1IE) TM1IE interrupt enable bit.

  0: disable TM1IE interrupt

  1: enable TM1IE interrupt

- Bits 4~7 Not used.
- Individual interrupt is enabled by setting its associated control bit in IOCF to "1".
- The IOCF Register could be read and written.

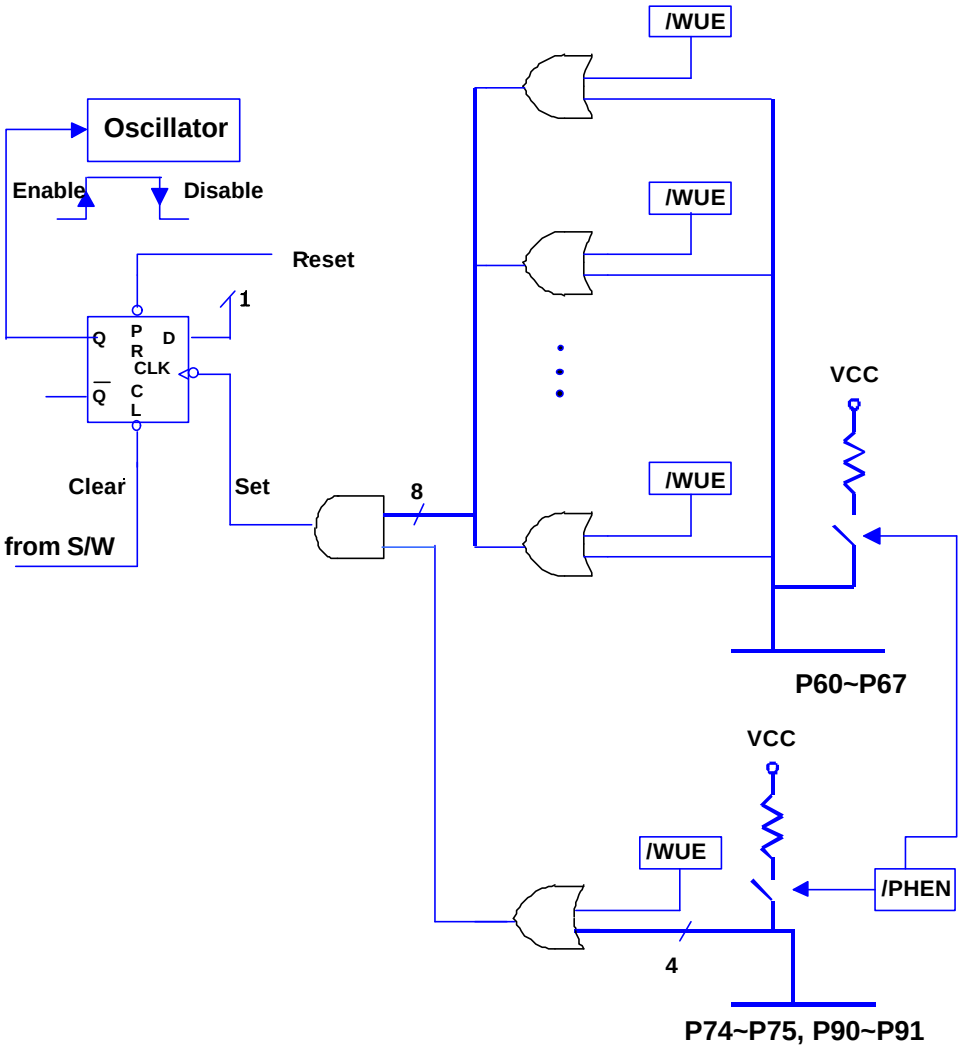


Fig. 5 Block Diagram of Sleep Mode and Wake-up Circuits on I/O Ports

4.3 TCC/WDT Presacler

An 8-bit counter is available as prescaler for the TCC or WDT. The prescaler is available for either the TCC or WDT only at any given time, and the PAB bit of CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the prescale ratio. The prescaler is cleared each time the instruction is written to TCC under TCC mode. The WDT and prescaler, when assigned to WDT mode, are cleared by the WDTC or SLEP instructions. Fig. 6 depicts the circuit diagram of TCC/WDT.

- R1(TCC) is an 8-bit timer/counter. TCC will increase by one at every instruction cycle (without prescaler).
- The watchdog timer is a free running on-chip RC oscillator. The WDT will keep running even when the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during the normal mode by software programming (if Code Option bit ENWDT is "1"). Refer to WDTE bit of IOCE register. Without presacler, the WDT time-out period is approximately 18 ms[1].

4.4 I/O Ports

The I/O registers, from Port 5 to Port 9, are bi-directional tri-state I/O ports. P60~P67, P74~P75, and P90~P91 provide the internal pull-high. P60~P67, P74~P75, and P90~P95 provide programmable wake-up function through software. P76~P77 can have an open-drain output by software control. P80~P81 are the R-option pins which are enabled by software. When the R-option function is used, it is recommended that P80 and P81 are use as output pins. During R-option enabled state, P80 and P81 must be programmed as input pins. If an external resistor is connected to P80 (P81) for the R-option function, the current consumption, if necessary, should be taken as an important factor in the applications for low power consideration.

The I/O ports can be defined as "input" or "output" pins by the I/O control registers (IOC5~IOC9) under program control. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig. 7. Note that the reading path source of input and output pins is different when reading the I/O port.

[1] NOTE: Vdd = 5V, set up time period = 16.2ms ± 5%
Vdd = 3V, set up time period = 18.0ms ± 5%

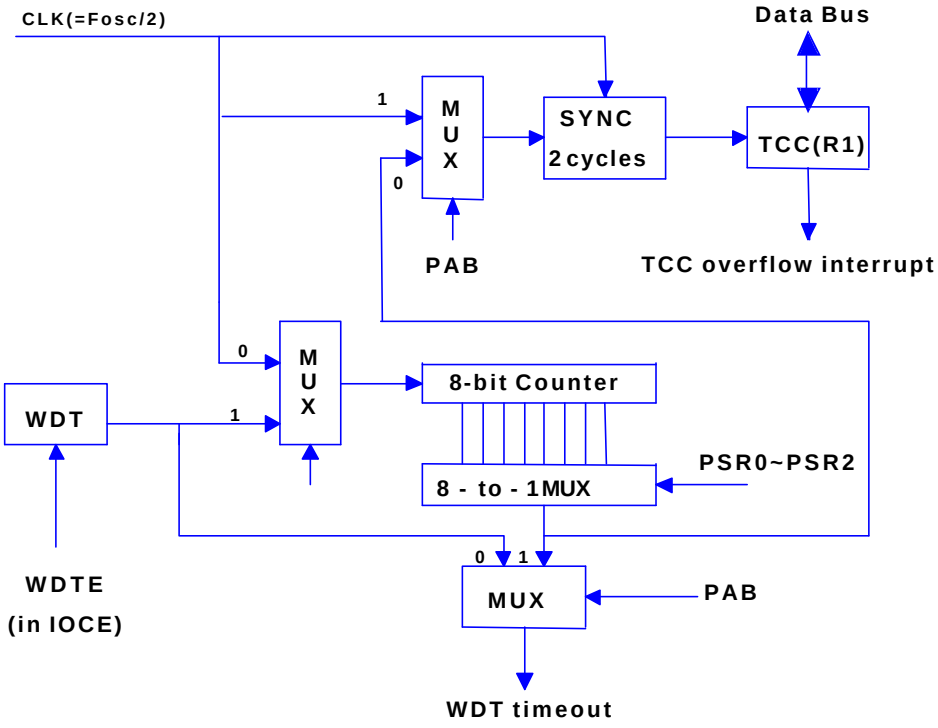


Fig. 6 Block Diagram of TCC WDT

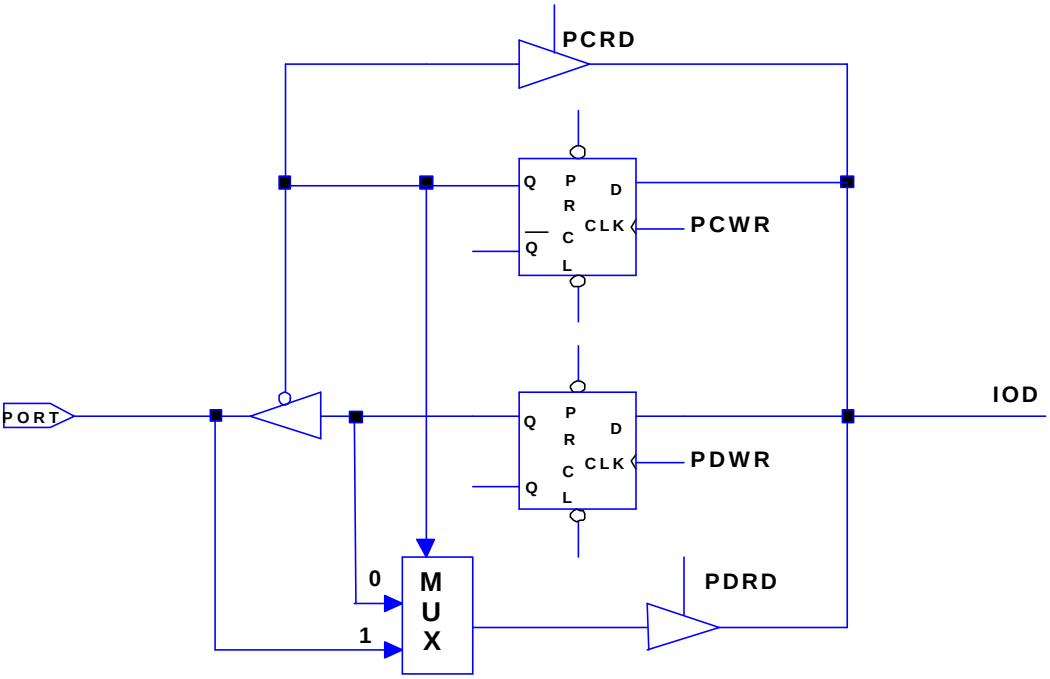


Fig. 7 (a) The Circuit of I/O Port and I/O Control Register

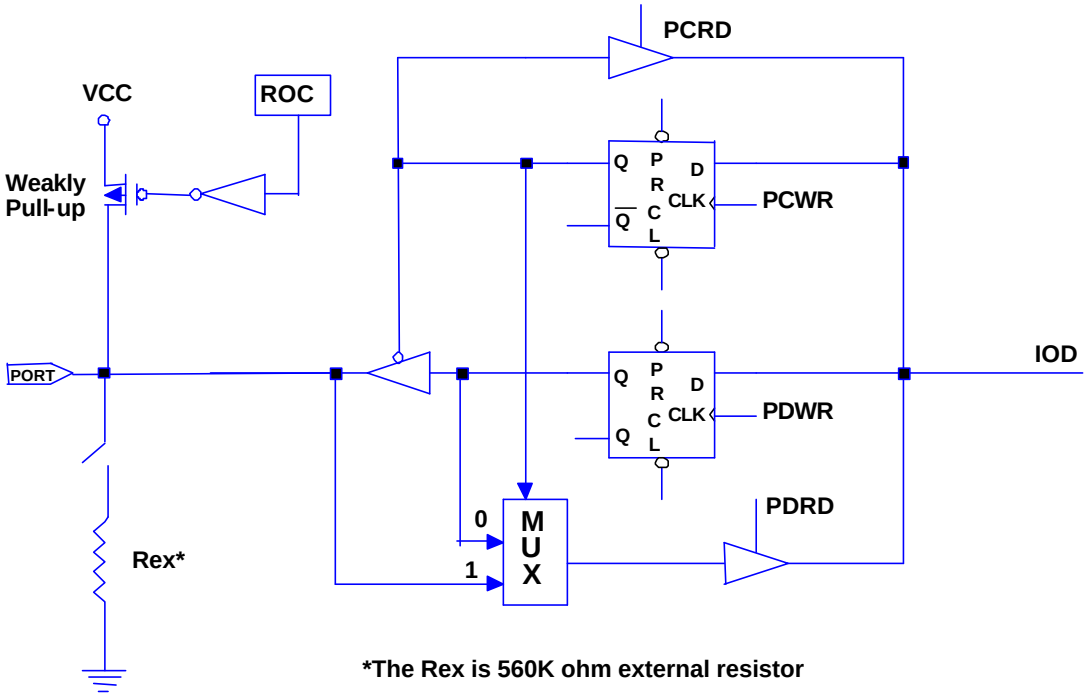


Fig. 7 (b) The Circuit of I/O Port with R-option (P80, P81)

4.5 SERIAL PERIPHERAL INTERFACE MODE

1. Overview & Features

Overview:

Figures 8, 9, and 10 show how EM78451 communicates with other devices through SPI module. If EM78451 is a master controller, it sends clock through the SCK pin. A couple of 8-bit data are transmitted and received at the same time. However, if EM78451 is defined as a slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted based on both the clock rate and the selected edge.

Features:

- Operation in either Master mode or Slave mode,
- Three-wire or four-wire synchronous communication; that is, full duplex
- Programmable baud rates of communication,
- Programming clock polarity, (RD bit7)
- Interrupt flag available for the read buffer full,
- Up to 8 MHz (maximum) bit frequency,

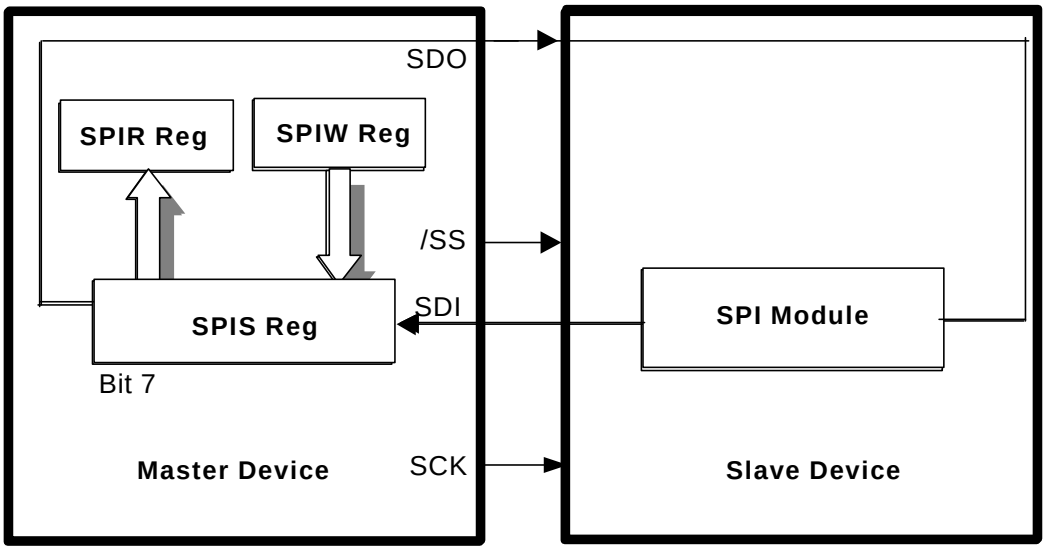


Fig. 8 SPI Master/Slave Communication

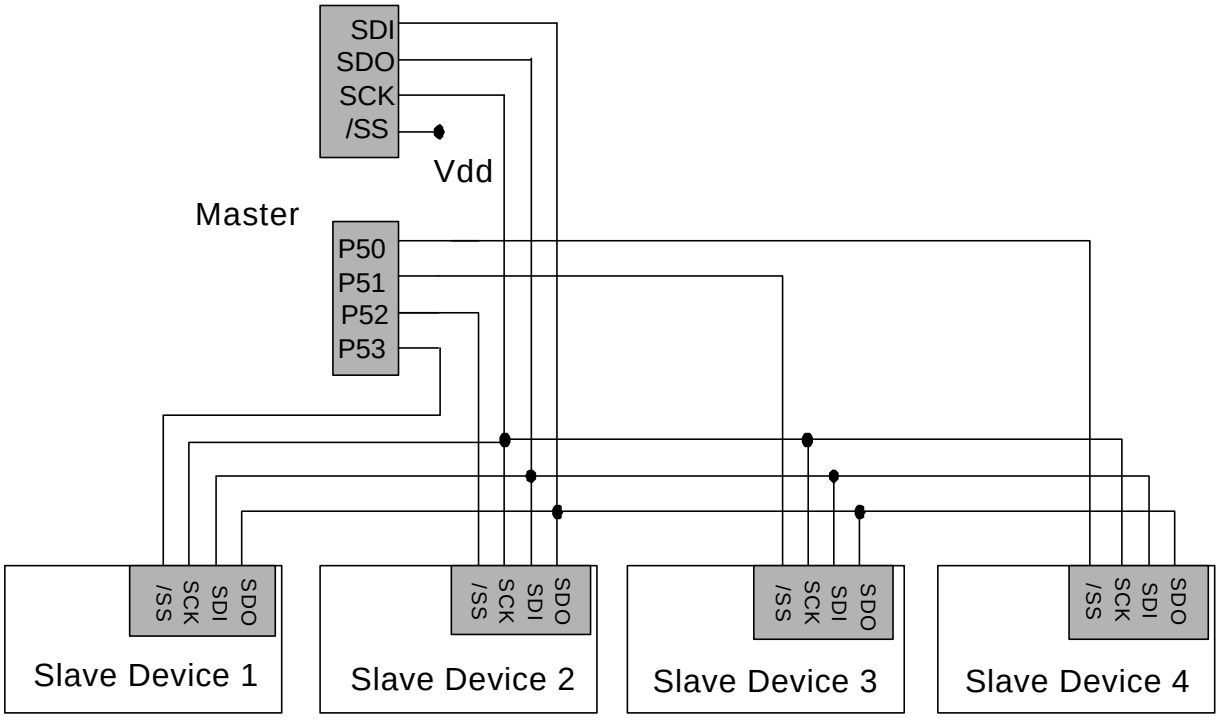


Fig. 9 The SPI Configuration of Single-Master and Multi-Slave

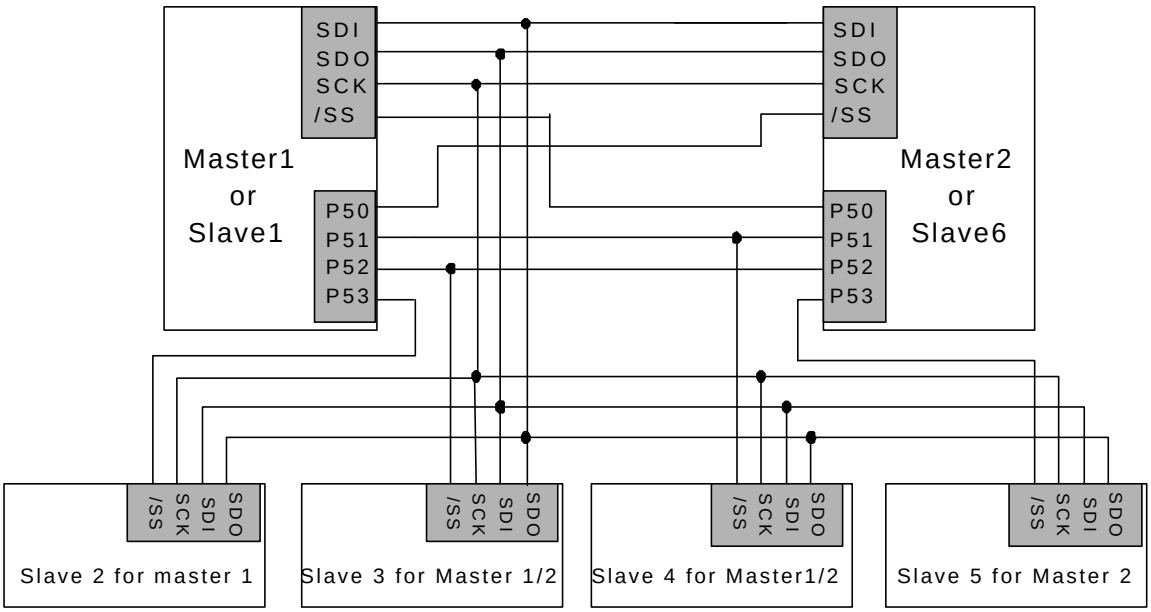


Fig. 10 The SPI Configuration of Single-Master and Multi-Slave

2. SPI Function Description

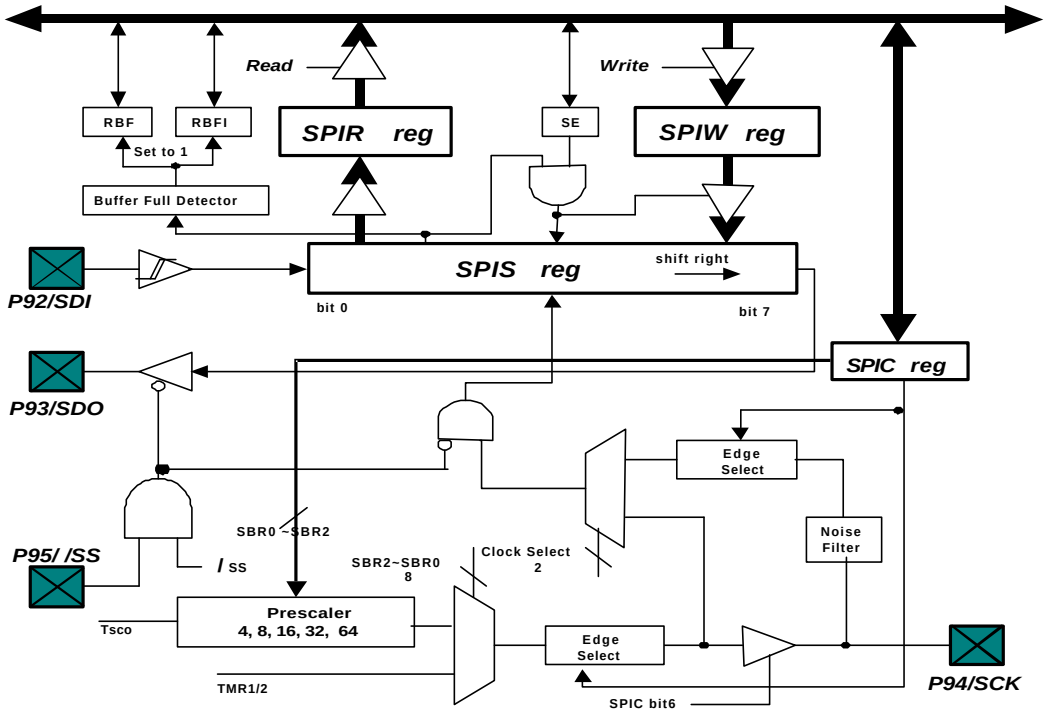


Fig. 11 SPI Block Diagram

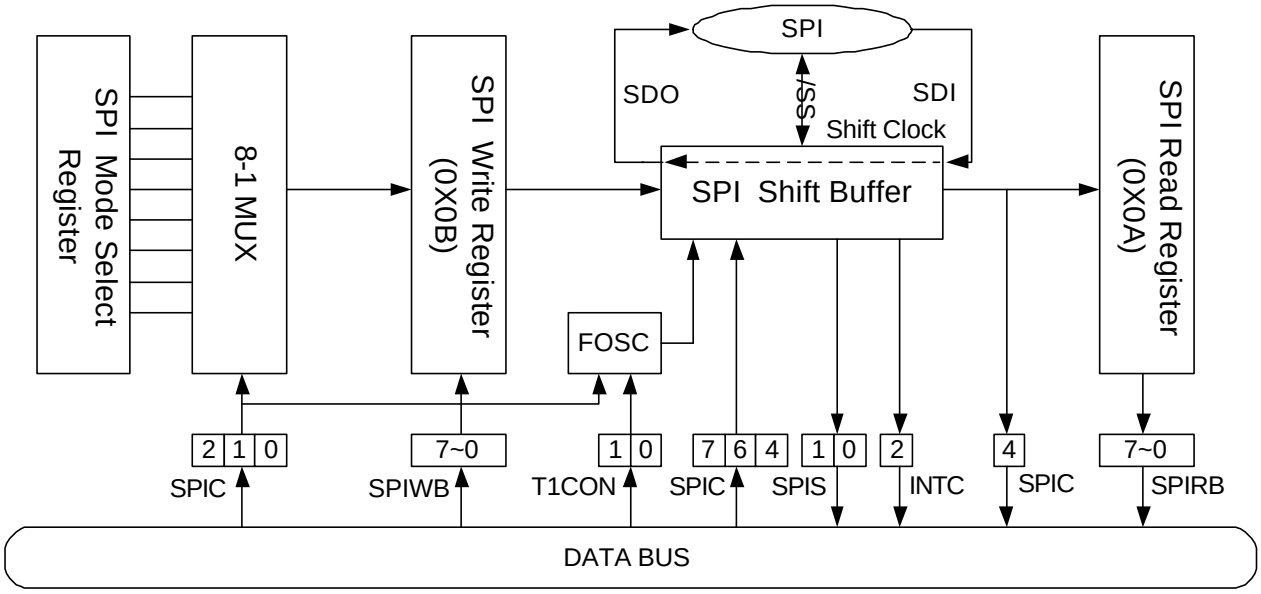


Fig. 12 The Function Block Diagram of SPI Transmission

The following describes the function of each block and explains how to carry out the SPI communication with the signals depicted in Fig.11 and Fig.12:

- **P92/SDI:** Serial Data In.
- **P93/SDO:** Serial Data Out.
- **P94/SCK:** Serial Clock.
- **P95//SS:** /Slave Select (Option). This pin (/SS) may be required during a slave mode.
- **RBF:** Set by Buffer Full Detector, and reset in software.
- **RBIF:** Set by Buffer Full Detector, and reset in software.
- **Buffer Full Detector:** Sets to 1, when an 8-bit shifting is complete.
- **SSE:** Loads the data in SPIS register, and begin to shift
- **SPIS reg.:** Shifting byte in and out. The MSB is shifted first. Both the SPIS register and the SPIW register are loaded at the same time. Once data are written, SPIS starts transmission / reception. The received data will be moved to the SPIR register, as the shifting of the 8-bit data is completed. The RBF (Read Buffer Full) flag and the RBFI (Read Buffer Full Interrupt) flag are then set.
- **SPIR** reg.: Read buffer. The buffer will be updated as the 8-bit shifting is completed. The data must be read before the next reception is finished. The RBF flag is cleared as the SPIR register reads.
- **SPIW** reg.: Write buffer. The buffer will deny any attempt to write until the 8-bit shifting is completed.

The SSE bit will be kept in 1 if the communication is still undergoing. This flag must be cleared as the

shifting is completed. Users can determine if the next write attempt is available.

- **SBRS2~SBRS0**: Programming the clock frequency/rates and sources.
- **Clock Select**: Selecting either the internal or external clock as the shifting clock.
- **Edge Select**: Selecting the appropriate clock edges by programming the CES bit

3. SPI Signal & Pin Description

The detailed functions of the four pins, SDI, SDO, SCK, and /SS, which are shown in Fig. 9, are as follows:

SDI/P92 (Pin 7):

- Serial Data In,
- Receive serially; the Most Significant Bit (MSB) first, the Least Significant Bit (LSB) last,
- Defined as high-impedance, if not selected,
- Program the same clock rate and clock edge to latch on both the master and slave devices,
- The received byte will update the transmitted byte,
- Both the RBF and the RBFIF bits (located in Register 0x0C) will be set as the SPI operation is completed.
- Timing is shown in Fig.13 and Fig. 14.

SDO/P93 (Pin 8):

- Serial Data Out,
- Transmit serially; the Most Significant Bit (MSB) first, the Least Significant Bit (LSB) last,
- Program the same clock rate and clock edge to latch on both the master and slave devices,
- The received byte will update the transmitted byte,
- The CES (located in Register 0x0D) bit will be reset, as the SPI operation is completed.
- Timing is shown in Fig.13 and 14.

SCK/P94 (Pin 9):

- Serial Clock
- Generated by a master device
- Synchronize the data communication on both the SDI and SDO pins
- The CES (located in Register 0x0D) is used to select the edge to communicate

- The SBR0~SBR2 (located in Register 0x0D) is used to determine the baud rate of communication
- The CES, SBR0, SBR1, and SBR2 bit have no effect in the slave mode
- Timing is show in Fig.13 and 14

/SS/P95 (Pin 10):

- Slave Select; negative logic,
- Generated by a master device to signify the slave(s) to receive data,
- Goes low before the first cycle of SCK appears and remains low until the last (eighth) cycle is completed,
- Ignores the data on the SDI and SDO pins when /SS is high, because the SDO is no longer driven.
- Timing is shown in Fig.13 and Fig. 14.

4. Programming the related registers

The related registers for defining SPI mode are shown in Table 2 and Table 3.

Table 2 Related Control Registers of the SPI Mode

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0D	*SPIC/RD	CES	SPIE	SRO	SSE	--	SBR2	SBR1	SBR0
0x0F	INTC/IOCF	--	--	--	--	TM1IE	SPIIE	EXIE	TCIE

- **SPIC:** SPI Control Register.
- **CES (bit 7):** Clock Edge Select bit

  1 = Data shifts out on falling edge, and shifts in on rising edge. Data is on hold during the high level.

  0 = Data shifts out on rising edge, and shifts in on falling edge. Data is on hold during the low level.
- **SPIE (bit 6):** SPI Enable bit

  1 = Enable SPI mode

  0 = Disable SPI mode
- **SRO (bit 5):** SPI Read Overflow bit

  1 **=** A new data is received while the previous data is still being on hold in the SPIB register. Under this condition, the data in SPIS register will be destroyed. To avoid setting this bit, users should read the SPIRB register even if the transmission is implemented only.

  0 **=** No overflow.

  <Note**>**: This can only occur under slave mode.

- **SSE (bit 4):**SPI Shift Enable bit

  1 **=** Start to shift, and stays on 1 while the current byte continues to transmit.

  0 = Reset as soon as the shifting is completed, and the next byte is ready to shift.

  <Note>**:** This bit can be reset by hardware only.

- **SBRS (bit 2~0):** SPI Baud Rate Select Bits

SBRS2 (Bit 2)	SBRS1 (Bit 1)	SBRS0 (Bit 0)	Mode	Baud Rate
0	0	0	Master	Fsco/2
0	0	1	Master	Fsco/4
0	1	0	Master	Fsco/8
0	1	1	Master	Fsco/16
1	0	0	Master	Fsco/32
1	0	1	Slave	/SS enable
1	1	0	Slave	/SS disable
1	1	1	Master	TMR1/2

<Note> In master mode, /SS is disable.

- **INTC:** Interrupt control register
- **Bit 3 (TM1IE)** TM1IE interrupt enable bit.

  0: disable TM1IE interrupt

  1: enable TM1IE interrupt

- **Bit 2 (SPIIE)** SPI interrupt enable bit.

  0: disable SPI interrupt

  1: enable SPI interrupt

- **Bit 1 (EXIE)** EXIF interrupt enable bit.

  0: disable EXIF interrupt

  1: enable EXIF interrupt

- **Bit 0 (TCIE)** TCIF interrupt enable bit.

  0: disable TCIF interrupt

  1: enable TCIF interrupt

Table 3 Related Status/data Registers of the SPI Mode

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0A	SPIRB/RA	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
0x0B	SPIWB/RB	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
0x0C	SPIS/RC	0	0	0	TM1IF	OD3	OD4	RBFIF	RBF

- **SPIRB:** SPI Read Buffer. Once the serial data is received completely, it will load to SPIRB from SPISR. The RBF bit and the RBFIF bit in the SPIS register will be set also.

- **SPIWB:** SPI Write Buffer. As a transmitted data is loaded, the SPIS register stands by and start to shift the data when sensing SCK edge with SSE set to "1".
- **SPIS:** SPI Status register
- **TM1IF(bit4):** Timer1 interrupt flag.
- **OD3 (bit 3):** Open-Drain Control bit (P93)

  1 **=** Open-drain enable for SDO,

  0 **=** Open-drain disable for SDO.
- **OD4 (bit 2):** Open-drain Control bit (P94)

  1 **=** Open-drain enable for SCK,

  0 **=** Open-drain disable for SCK.
- **RBFIF (bit 1):** Read Buffer Full Interrupt flag

1 **=** Receive is completed, SPIB is full, and an interrupt occurs if enabled.

0 **=** Receive is ongoing, SPIB is empty.

- **RBF (bit 0):** Read Buffer Full flag

1 **=** Receive is completed, SPIB is full.

0 **=** Receive is ongoing, SPIB is empty.

5. SPI Mode Timing

The edge of SCK is selected by programming bit CES. The waveform shown in Fig.13 is applicable regardless of whether the EM78451 is under master or slave mode with /SS disabled. However, The waveform in Fig. 14 can only be implemented in slave mode with /SS enabled.

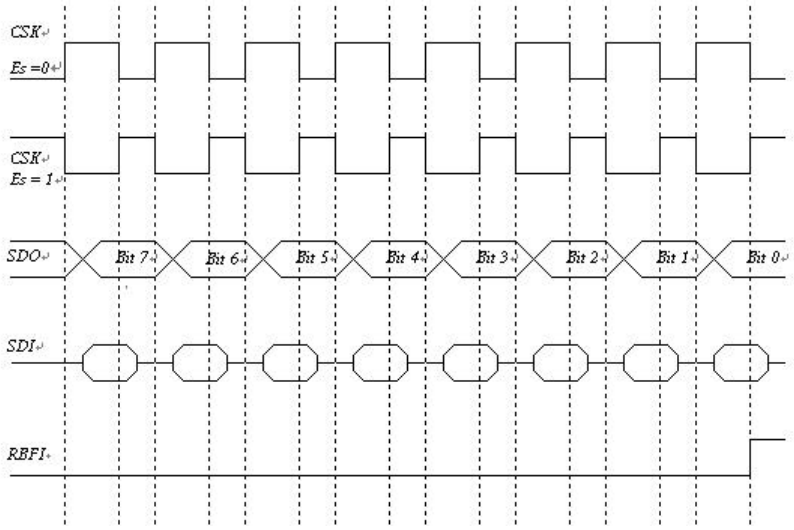


Fig. 13 SPI Mode with /SS Disable

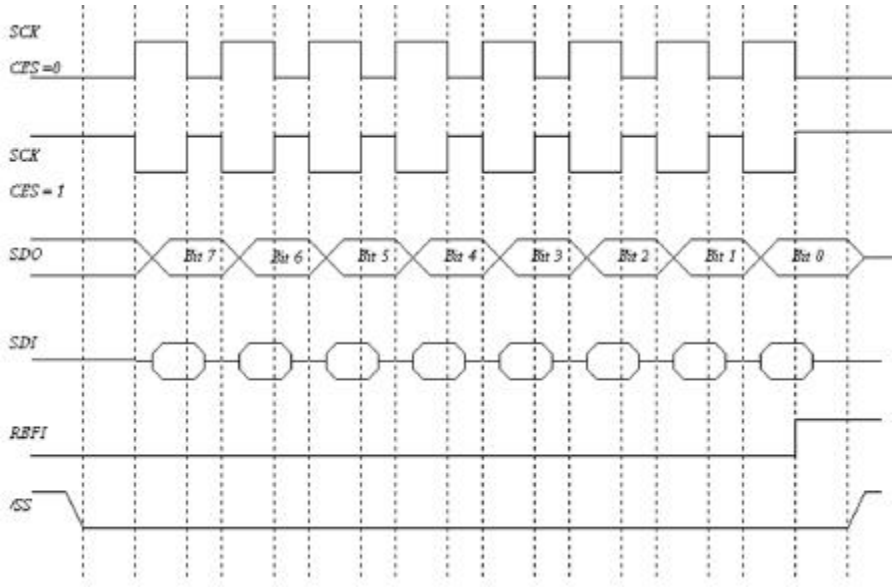


Fig. 14 SPI Mode with /SS Enable

6. Software Application of SPI

Example for SPI:

For Master

```
ORG 0X0
  SETTING:
  CLRA
  IOW 0X05              ;SET PORT5 OUTPUT
  IOW 0X06              ;SET PORT6 OUTPUT
  MOV 0X05,A
  MOV A,@0B11001111     ;SET PRESCALER FOR WDT
  CONTW
  MOV A,@0B00010001     ;DISABLE WAKEUP FUNCTION
  IOW 0X0E
  MOV A,@0B00000000     ;DISABLE INTERRUPT
  IOW 0X0F
  MOV A,@0x07           ;SDI INPUT AND SDO, SCK OUTPUT
  IOW 0x09
```

```
    MOV A,@0B10000000  ;CLEAR RBF AND RBFIF FLAG
    MOV 0x0C,A
    MOV A,@0B11100000  ;SELECT CLOCK EDGE AND ENABLE SPI
    MOV 0X0D,A
    START:
    WDTC
    BC 0X0C,1          ;CLEAR RBFIF FLAG
    MOV A,@0XFF
    MOV 0X05,A         ;SHOW A SIGNAL AT PORT5
    MOV 0X0A,A         ;MOVE FF AT READ BUFFER
    MOV A,@0XAA        ;MOVE AA AT WRITE BUFFER
    MOV 0X0B,A
    BS 0X0D,4          ;START TO SHIFT SPI DATA
    NOP
    JBC 0X0D,4         ;POLLING LOOP FOR CHECKING SPI TRANSMISSION COMPLETED
    JMP $-2
    BC 0X03,2
    CALL DELAY         ;TO CATCH THE DATA FROM SLAVER
    MOV A,0X0A
    XOR A,@0X5A        ;COMPARE THE DATA FROM SLAVER
    JBS 0X03,2
    JMP START
FLAG:
    MOV A,@0X55        ;SHOW THE SIGNAL WHEN RECEIVING CORRECT DATA FROM SLAVER
    MOV 0X05,A
    CALL DELAY
    JMP START
DELAY:
                       ; (USER'S PROGRAM)
    EOP
    ORG 0XFFF
    JMP SETTING
```

For Slaver

```
ORG 0X0
INITI:
   JMP INIT
   ORG 0X2
INTERRUPT:              ;INTERRUPT ADDRESS
   MOV A,@0X55
   MOV 0X06,A           ;SHOW A SIGNAL AT PORT 6 WHEN ENTERING INTERRUPT
   MOV A,@0B11100110    ;ENABLE SPI, /SS DISABLED
   MOV 0X0D,A
   BS 0X0D,4            ;KEEP SSE AT 1 TO WAIT FOR SCK SIGNAL IN ORDER TO SHIFT DATA
   MOV A,@0X00          ;MOVE 00 TO WRITE BUFFER IN ORDER TO KEEP MASTER'S READ BUFFER AS 00
   MOV 0X0B,A
   BS 0X0D,4            ;KEEP SSE AT 1 TO WAIT FOR SCK SIGNAL IN ORDER TO SHIFT DATA
   NOP
   JBC 0X0D,4           ;POLLING LOOP FOR CHECKING SPI TRANSMISSION COMPLETED
   JMP $-2
   BS 0X0D,4            ;KEEP SSE AT 1 TO WAIT FOR SCK SIGNAL IN ORDER TO SHIFT DATA
   BC  0X03,2
   MOV A,0X0A
   MOV 0X06,A           ;READ MASTER'S DATA FROM READ BUFFER
   XOR A,@0XAA          ;CHECK PASS SIGNAL FROM READ BUFFER
   JBS 0X03,2
   JMP $-6
   JMP SPI

ORG 0X30
INIT:
   CLRA
   IOW 0X05
   IOW 0X06
   MOV 0x05,A
   MOV 0X06,A
```

```
    MOV A,@0XFF
    IOW 0X08
    MOV A,@0B11001111  ;SET PRESCALER FOR WDT
    CONTW
    MOV A,@0B00010001  ;DISABLE WAKEUP FUNCTION
    IOW 0X0E
    MOV A,@0B00000010  ;ENABLE EXTERNAL INTERRUPT
    IOW 0XF
    ENI
    MOV A,@0B00110111
    IOW 0x09
    BC  0X3F,1         ;CLEAR RBFIF FLAG
    NOP
    JBS 0X3F,1         ;POLLING LOOP FOR CHECKING INTERRUPT OCCURENCE
    JMP $-2
    JMP INTERRUPT
SPI:
    BS 0X0D,4          ;KEEP SSE ENABLED AS LONG AS POSSIBLE
    WDTC
    MOV A,@0X0F        ;SHOW A SIGNAL WHEN ENTERING SPI LOOP
    MOV 0X06,A
    JBC 0X08,1         ;CHOOSE P81 AS A SIGNAL BUTTON
    JMP SPI
    MOV A,@0X5A        ;MOVE 5A INTO WRITE BUFFER WHEN P81 BUTTON IS PUSHED
    MOV 0X0B,A
    NOP
    JBC 0X0D,4         ;POLLING LOOP FOR CHECKING SPI TRANSMISSION COMPLETED
    JMP $-2
    BS 0XD,4
    NOP
    NOP
    MOV A,@0XF0        ;DISPLAY AT PORT6 WHEN P81 BUTTON IS PUSHED
    MOV 0X06,A
    MOV A,@0X00        ;SEND A SIGNAL TO MASTER TO PREVENT INFINITE LOOP
```

```
    MOV 0X0B,A
    NOP
    JBC 0X0D,4
    JMP $-2
    BS 0X0D,4
    BS 0x0C,7
    BC 0x0C,1
    NOP
    JMP SPI
DELAY:
                    ; (USER' S PROGRAM)
    EOP
    ORG 0XFFF
    JMP INITI
```

4.6 Timer 1

1. Overview

Timer1(TMR1) is an eight-bit clock counter with a programmable prescaler. It is designed for the SPI module as a baud rate clock generator. TMR1 can be read and written and cleared on any reset conditions. If employed, it can be turned down for power saving by setting TMR1EN bit [T1CON<2>] to 0.

2. Function description

Fig. 15 shows TIMER1 block diagram. Each signal and block is described as follows:

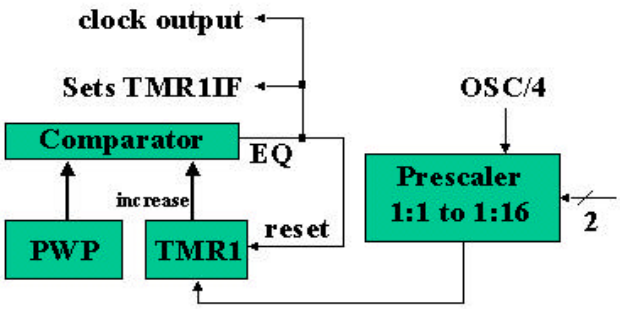


Fig. 15 TIMER1 Block Diagram

- **OSC/4**: Input clock.
- **Prescaler**: Option of 1:1, 1:4, 1:8, and 1:16 defined by T1P1 and T1P02(T1CON<1, 0>).It is cleared when a value is written to TMR1 or T1CON, and during any kind of reset as well.
- **PWP**: Pulse width preset register; The desired width of baud clock is written in advance.
- **TMR1**: Timer 1 register; TMR1 increases until it matches with PWP, and then resets to 0. If it is chosen optionally in the SPI mode, its output is fed as a shifting clock.
- **Comparator:** To change the output status while a match occurs. The TMR1IF flag will be set at the same time.

3. Programmed the related registers

The related registers for defining TMR1 are shown in Table 4 and Table 5

Table 4 Related Control Registers of the TMR1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	SPIS/RC	0	0	0	TM1IF	OD3	OD4	RBFIF	RBF
0x0F	INTC/IOCF	0	0	0	0	TM1IE	SPIIE	EXIE	TCIE

Table 5 Related Status/Data Registers of TMR1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0E	TMR1/RE	TMR17	TMR16	TMR15	TMR14	TMR13	TMR12	TMR11	TMR10
0x0F	PWP/RF	PWP7	PWP6	PWP5	PWP4	PWP3	PWP2	PWP1	PWP0
0x0C	T1CON/IOCC	0	0	0	0	0	TM1E	TM1P1	TM1P0

- TMR1: Timer1 Register

  TMR17~TMR10 is bit set of Timer1 register and it increases until the value matches PWP and then it reset to 0.

- PWP: Pulse Width Preset Register

  PWP7~PWP0 is bit set of pulse width preset for the desire width of baud clock in advance.

- T1CON: Timer1 Control Register

  TM1E (bit2): Timer1 enable bit

  TM1P1 and TM1P0 (bit1~0): Timer1 prescaler for FSCO

TM1P1	TM1P0	Prescaler Rate
0	0	1:1
0	1	1:4
1	0	1:8
1	1	1:16

4.7 RESET and Wake-up

A RESET is initiated by

(1) Power on reset, or

(2) WDT timeout. (if enabled)

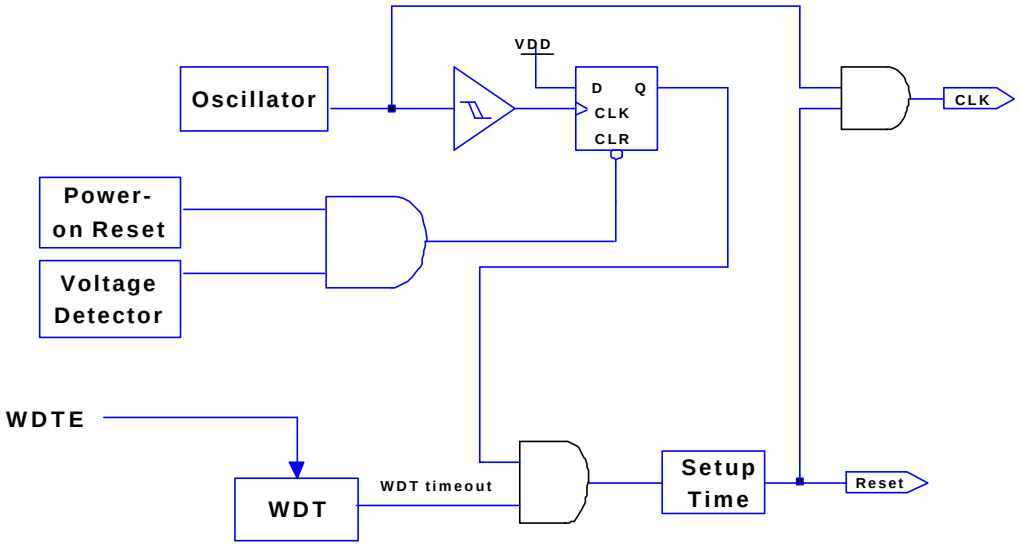


Fig. 16 Block Diagram of Reset

The device is kept in a RESET condition for a period of approx. 18ms[1] (one oscillator start-up timer period) after the reset is detected and Fig.16 is the block diagram of reset. Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "1".
- When power is switched on, bits 5~6 of R3 and the upper 2 bits of R4 are cleared.
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- The Watchdog timer is enabled if Code Option bit ENWDT is "1".
- The CONT register is set to all "1" except bit 6 (INT flag).
- Bits 3,6 of IOCE register are cleared, bits 0,4~5 of IOCE register are set to "1".

[1] NOTE: Vdd = 5V, set up time period = 16.2ms ± 5%
Vdd = 3V, set up time period = 18.0ms ± 5%

- Bits 0 of R3F and bits 0 of IOCF registers are cleared.

The sleep mode (power down) is achieved by executing the SLEP instruction (named as SLEEP1 MODE). While entering sleep mode, the WDT (if enabled) is cleared but keeps on running. The controller is awakened by WDT timeout (if enabled), and it will cause the controller to reset. The T and P flags of R3 are used to determine the source of the reset (wake-up).

In addition to the basic SLEEP1 MODE, EM78451 has another sleep mode (caused by clearing "SLPC" bit of IOCE register, designated as SLEEP2 MODE). In the SLEEP2 MODE, the controller can be awakened by

(a) Any one of the wake-up pins is set to "0." (refer to Fig.17). Upon waking, the controller will continue to execute the program in-line. In this case, before entering SLEEP2 MODE, the wake-up function of the trigger sources (P60~P67, P74~P75, and P90~P91)should be selected (e.g. input pin) and enabled (e.g. pull-high, wake-up control). One caution should be noted is that after waking up, the WDT is enabled if Code Option bit ENWDT is "1". The WDT operation (to be enabled or disabled) should be appropriately controlled by software after waking up.

(b) WDT time-out (if enabled). On wake-up, will cause the controller to reset.

Table 6 The Summary of the Initialized Values for Registers

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC7	Bit Name	C77	C76	C75	C74	C73	C72	C71	C70
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC8	Bit Name	C87	C86	C85	C84	C83	C82	C81	C80
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC9	Bit Name	C97	C96	C95	C94	C93	C92	C91	C90
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	/PHEN	/INT	-	-	PAB	PSR2	PSR1	PSR0
		Power-On	1	0	1	1	1	1	1	1
		/RESET and WDT	1	P	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0(IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

0x01	R1(TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2(PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	**P	**P	**P	**P	**P	**P	**P	**P
0x03	R3(SR)	Bit Name	GP	PS1	PS0	T	P	Z	DC	C
		Power-On	0	0	0	t	t	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-Up from Pin Change	P	P	P	t	t	P	P	P
0x04	R4(RSR)	Bit Name	RSR.1	RSR.0	-	-	-	-	-	-
		Power-On	0	0	U	U	U	U	U	U
		/RESET and WDT	0	0	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x05	R5(P5)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x06	R6(P6)	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x07	R7(P7)	Bit Name	P77	P76	P75	P74	P73	P72	P71	P70
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x08	R8(P8)	Bit Name	P87	P86	P85	P84	P83	P82	P81	P80
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x09	R9(P9)	Bit Name	P97	P96	P95	P94	P93	P92	P91	P90
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0A	RA(SPIRB)	Bit Name	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0B	RB(SPIWB)	Bit Name	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0C	RC(SPIS)	Bit Name	ENSDO	OBDC	IBDC	TIIF	OD3	OD4	RBFIF	RBF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0D	RD(SPIC)	Bit Name	CES	SPIE	SRO	SPISE	-	SBRS2	SBRS1	SBRS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0E	RE(TMR1)	Bit Name	TMR17	TMR16	TMR15	TMR14	TMR13	TMR12	TMR11	TMR10
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0F	RF(PWP)	Bit Name	PWP7	PWP6	PWP5	PWP4	PWP3	PWP2	PWP1	PWP0
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1

		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x3F	R3F(ISR)	Bit Name	-	-	-	-	T1IF	SPIIF	EXIF	TCIF
		Power-On	U	U	U	U	0	0	0	0
		/RESET and WDT	U	U	U	U	0	0	0	0
		Wake-Up from Pin Change	U	U	U	U	P	P	P	P
0x0C	IOCC	Bit Name	-	-	-	-	-	T1E	T1P1	T1P0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0D	IOCD	Bit Name	S7	-	-	-	/PU9	/PU8	/PU6	/PU5
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0E	IOCE	Bit Name	-	ODE	WTE	SLPC	ROC	-	-	/WUE
		Power-On	U	0	1	1	0	U	U	1
		/RESET and WDT	U	0	1	1	0	U	U	1
		Wake-Up from Pin Change	U	P	1	1	P	U	U	P
0x0F	IOCF	Bit Name	-	-	-	-	T1IE	SPIIE	EXIE	TCIE
		Power-On	U	U	U	U	0	0	0	0
		/RESET and WDT	U	U	U	U	0	0	0	0
		Wake-Up from Pin Change	U	U	U	U	P	P	P	P
0x10~0x3E	GPR	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

** To execute the next instruction after the "SLPC" bit status of IOCE register being on high-to-low transition.

X: Not used. U: Unknown or don't care. P: Previous value before reset. t: Check Table 7

The Status of RST, T, and P of STATUS Register

A RESET condition is initiated by the following events:

1. A power-on condition,
2. Watchdog timer time-out.

The values of T and P, listed in Table 7 are used to check how the processor wakes up.

Table 8 shows the events that may affect the status of T and P.

Table 7 The Values of RST, T and P After RESET

Reset Type	T	P
Power on	1	1
WDT during Operating mode	0	P
WDT wake-up during SLEEP1 mode	0	0
WDT wake-up during SLEEP2 mode	0	P
Wake-Up on pin change during SLEEP2 mode	P	P

*P: Previous status before reset

Table 8 The Status of RST, T and P Being Affected by Events

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-Up on pin change during SLEEP2 mode	P	P

*P: Previous value before reset

4.8 Interrupt

The EM78451 has the following interrupts.

1. TCC overflow interrupt
2. External interrupt (/INT)
3. Serial Peripheral Interface (SPI) transmission completed interrupt.
4. Timer1 comparator completed interrupt.

R3F is the interrupt status register, which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (if enabled) is generated, will cause the next instruction to be fetched from address 001H. Once in the interrupt service routine the source of the interrupt can be determined by polling the flag bits in the R3F register. The interrupt flag bit must be cleared by software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

The flag in the Interrupt Status Register (R3F) is set regardless of the status of its mask bit or the execution of ENI instruction. Note that reading R3F will obtain the output of logic AND of R3F and IOCF (refer to Fig. 17). The RETI instruction exits interrupt routine and enables the global interrupt (execution of ENI instruction).

When an interrupt is generated by INT instruction (if enabled), it causes the next instruction to be fetched from address 002H.

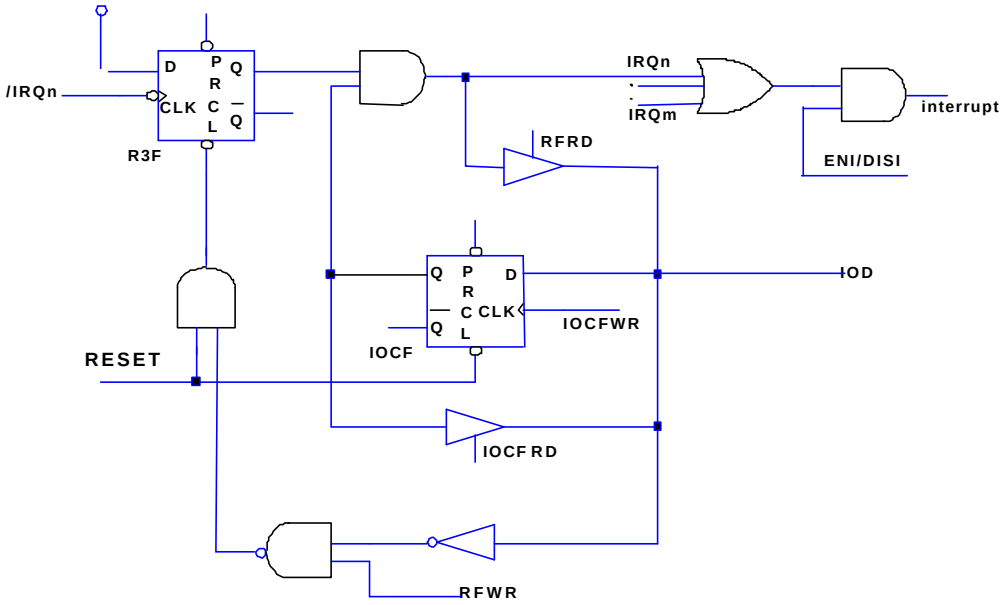


Fig. 17 Interrupt input circuit

4.9 Oscillator

1. Oscillator Modes

The EM78451 can operate in four different oscillator modes. There are high XTAL (HXT) oscillator mode, low XTAL (LXT) oscillator mode, External RC oscillator mode(ERC), and Internal C、External R oscillator mode. User can select one of them by programming MS, RCT, IRC, HLF and HLP in the Code Option Register. Table 9 depicts how these three modes are defined.

Table 9 Oscillator Modes by MS, IRC, RCT.

Mode	MS	IRC	RCT	HLF
High XTAL Oscillator	1	X	X	1
Low XTAL Oscillator	1	X	X	0
External RC Oscillator	0	1	1	X
External R and Internal C Oscillator	0	1	0	X

<Note> X: Don’ t care

2. Crystal Oscillator/Ceramic Resonators (XTAL)

EM78451 can be driven by an external clock signal through the OSCI pin as shown in Fig 18. In most applications, pin OSCI and pin OSCO is connected with a crystal or ceramic resonator to generate oscillation. Fig 19 depicts such circuit. Table 10 provides the recommends values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1

and C2. RS, a serial resistor may be necessary for AT strip cut crystal or low frequency mode.

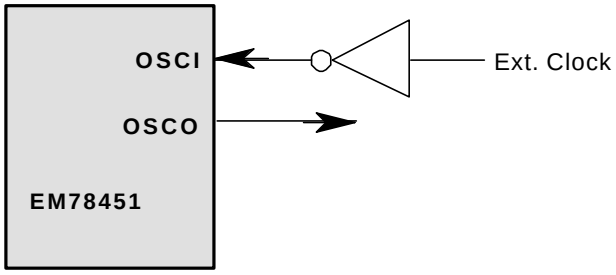


Fig. 18 Circuit for External Clock Input

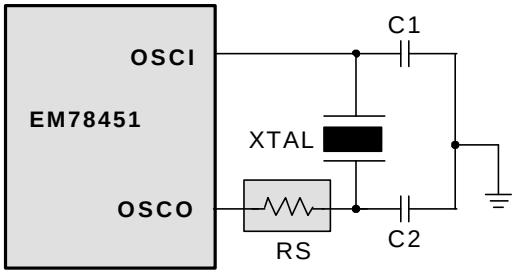


Fig. 19 Circuit for Crystal/Resonator

Table 10 Capacitor Selection Guide for Crystal Oscillator Ceramic Resonators

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonator	HXT	455 KHz	10~150	10~150
		1.0 MHz	40~80	40~80
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768 KHz	25	15
		100 KHz	25	25
		200 KHz	25	25
	HXT	455 KHz	20~40	20~150
		1.0 MHz	15~30	15~30
		2.0 MHz	15	15
		4.0 MHz	15	15

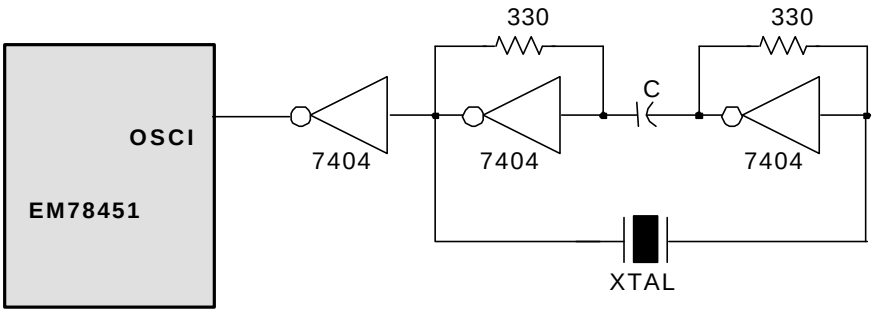


Fig. 20 Circuit for Crystal/Resonator-Series Mode

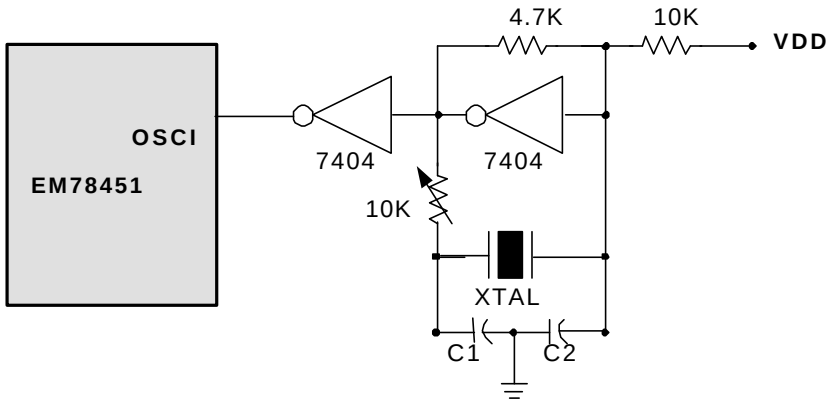


Fig. 21 Circuit for Crystal/Resonator-Parallel Mode

3. RC Oscillator Mode

For some applications that do not need a very precise timing calculation, the RC oscillator (Fig 22 & Fig 23) offers a lot of cost savings. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to the manufacturing process variation.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and that the the value of Rext should not be greater than 1 M ohm. If they cannot be kept in this range, the frequency is easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator becomes unstable because the NMOS cannot properly discharge the current of the capacitor.

Based on the above reasons, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types, and the way the PCB is layout, will affect the system frequency.

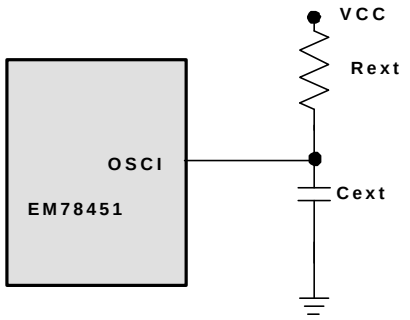


Fig. 22 Circuit for External RC Oscillator Mode

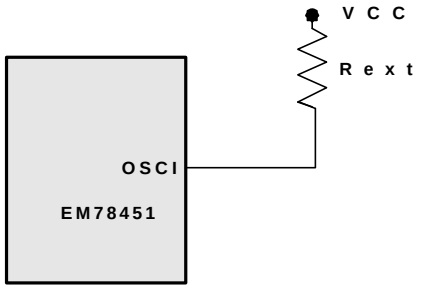


Fig. 23 Circuit for External R, Internal C Oscillator Mode

Calibrate frequency of External RC oscillator (For reference only)

C ext	R ext	Fosc @5.0V,25℃
20pF	3.3K	3.4MHz
	5.1K	2.2MHz
	10K	1.3MHz
	100K	144KHz
100pF	3.3K	1.39MHz
	5.1K	935KHz
	10K	500KHz
	100K	54.5KHz
300pF	3.3K	740KHz
	5.1K	490KHz
	10K	255KHz
	100K	28KHz

Internal C, external R Table (For reference only)

External R (Ohm)	Fosc @5.0V, 25℃ (Hz)
10K	12M
15K	7.7M
20K	5.7M
30K	3.65M
51K	2.24M
100K	1.14M
150K	749K
200K	559K
510K	214K
2M	56K
3.3M	32.8K

4.10 Code Option Register

0	1	2	3	4	5	6
ENWDT	MS	HLF	LVDD	RCT	DEL1	DEL0

Bit 0 (ENWDT): Watchdog Timer control.

1: Enable

0: Disable

• Bit 1 (MS): Oscillator type.

1: XTAL type

0: RC type

• Bit 2 (HLF): Frequency mode.

1: High frequency (>32.768KHz)

0: Low frequency (=32.768KHz)

• Bit 3 (LVDD): Levels of the operating voltage.

1: 2.3V~4V

0: 4V~5.5V

• Bit 4 (RCT): RC type.

1: External RC

0: Internal RC

• Bit 5 (DEL1) and Bit 6 (DEL0): Speed of SPI.

DEL 1	DEL 0	Speed (MHz)	Delay time (ns)	Use Type
0	0	8	0 ns	Not use SPI mode

0	1	2.5	50 ns	
1	0	1	100 ns	
1	1	Not use		Not use

*Do not set DEL1 and DEL0 bits to all "1", otherwise, the microprocessor won't work.

• The test code of EM78451

The following program must be added in order to heighten the liability of the mass production. The test code must not be executed during free running.

Address	Code	Statement
FFA	0006	IOW 0x06
FFB	0546	INC 0x06
FFC	01C6	DEC 0x06
FFD	01C5	DEC 0x05
FFE	0000	NOP

4.11 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. All instructions are executed within one single instruction cycle (consisting of 2 oscillator periods), unless the program counter is changed by-

(a) Executing the instruction "MOV R2,A", "ADD R2,A", "TBL", or any other instructions that write to R2 (e.g. "SUB R2,A", "BS R2,6", "CLR R2", ···).

(b) Executing CALL, RET, RETI, RETL, JMP, Conditional skip (JBS, JBC, JZ, JZA, DJZ, DJZA) whuch were tested to be true.

Under these cases, the execution takes two instruction cycles.

In addition, the instruction set has the following features:

(1). Every bit of any register can be set, cleared, or tested directly.

(2). The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The symbol "R" represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator that selects the value for the bit, located in the register "R" and affects by the operation. "k" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None <Note1>
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None <Note1>
0 0000 0010 0000	0020	TBL	R2+A → R2, Bits 8~9 of R2 unchanged	Z,C,DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None <Note2>
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None <Note3>

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1 1110 0000 0010	1E02	INT	PC+1 → [SP], 002H → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC

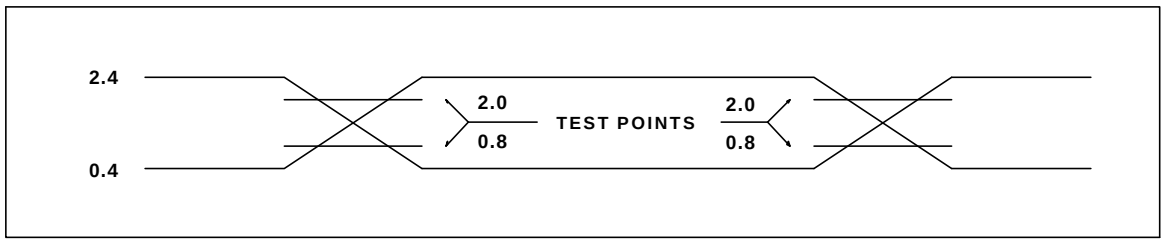
<Note1> This instruction is applicable to IOC5 ~ IOC9, IOCD~IOCF only.

<Note2> This instruction is not recommended for RF operation.

<Note3> This instruction cannot operate on R3F.

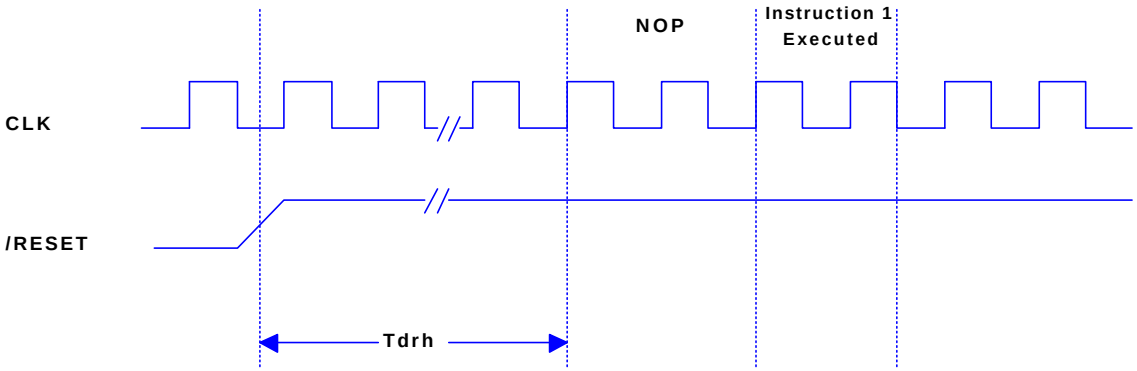
4.12 Timing Diagrams

AC Test Input/Output Waveform

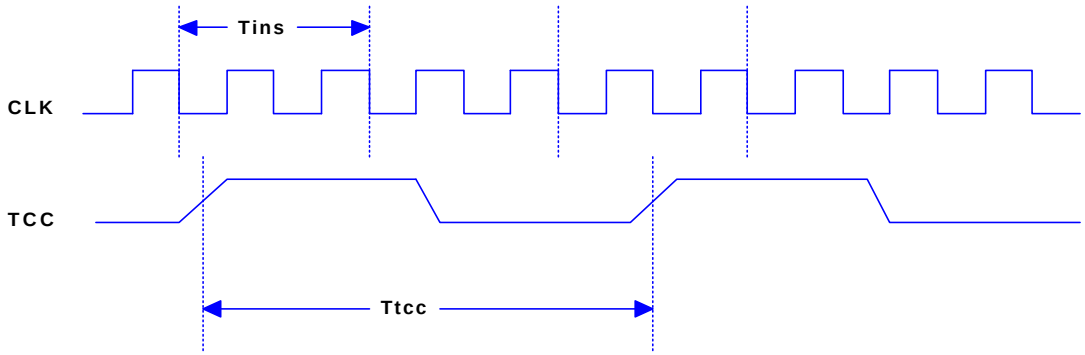


AC Testing : Input is driven at 2.4V for logic "1",and 0.4V for logic "0".Timing measurements are made at 2.0V for logic "1",and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")



5. ABSOLUTE MAXIMUM RATING

Items	Rating		
Temperature under bias	0°C	to	70°C
Storage temperature	-65°C	to	150°C
Input voltage	-0.3V	to	+6.0V
Output voltage	-0.3V	to	+6.0V
Operating Frequency (2clk)	DC	to	20MHz

6. ELECTRICAL CHARACTERISTICS

(1) DC Characteristic

(Ta=0°C~70°C, VDD=5V±5%, VSS=0V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
FXT	XTAL VDD to 2.3V	Two clocks	DC		4	MHz
	XTAL VDD to 3V		DC		8	
	XTAL VDD to 5V		DC		20	
FRC	RC VDD to 2.3V	Two clocks	DC		4	MHz
	RC VDD to 3V		DC		4	
	RC VDD to 5V		DC		4	
IIL	Input Leakage Current	VIN = VDD, VSS			±1	μA
VIH1	Input High Voltage VDD=5V)		2.0			V
VIL1	Input Low Voltage (VDD=5V)				0.8	V
VIHX1	Clock Input High Voltage (VDD=5V	OSCI	2.5			V
VILX1	Clock Input Low Voltage (VDD=5V	OSCI			1.0	V
VIH2	Input High Voltage(VDD=3V)		1.5			V
VIL2	Input Low Voltage (VDD=3V)				0.4	V
VIHX2	Clock Input High Voltage (VDD=3V)	OSCI	1.5			V
VILX2	Clock Input Low Voltage (VDD=3V)	OSCI			0.6	V
VOH1	Output High Voltage (Ports 5,6,8, P74~P77, P90~P92,P95~P97,and PF5~PF7)	IOH = -8.0mA	2.4			V
VOH2	Output High Voltage (P70~P72)	S7=1(IOCD Register bit7), IOH = -7.0mA	2	2.4		V
		S7=0(IOCD Register bit7), IOH = -7.0mA	2.4			
VOH3	Output High Voltage (P93/SDO,P94/SCK)	IOH = -5.0mA	2.4			V
VOL1	Output Low Voltage (Ports 5,6,8, P74~P77, P90~P92,P95~P97,and PF5~PF7))	IOL = 5.0mA			0.4	V
VOL2	Output Low Voltage (P70~P72)	S7=1(IOCD Register bit7), IOH = 10.0mA		0.4	0.8	V
		S7=0(IOCD Register bit7), IOH = 10.0mA			0.4	
VOL3	Output Low Voltage (P93/SDO, P94/SCK)	IOL = 7.0mA			0.4	V

VOL4	Output Low Voltage (P74~P77)	IOL = 15.0mA			0.4	
IPH	Pull-high current	Pull-high active, input pin at VSS	-50	-100	-240	µA
IPH2	Pull-high current (P74,P75)	Pull-high active, input pin at VSS		1		mA
ISB	Power down current	All input and I/O pin at VDD, output pin floating, WDT enabled			10	µA
ICC	Operating supply current	/RESET="High", Fosc=1.84324MHz (CK2="0"), output pin floating			3	mA

(2) AC Characteristic

(Ta=0°C~70°C, VDD=5V±5%, VSS=0V)

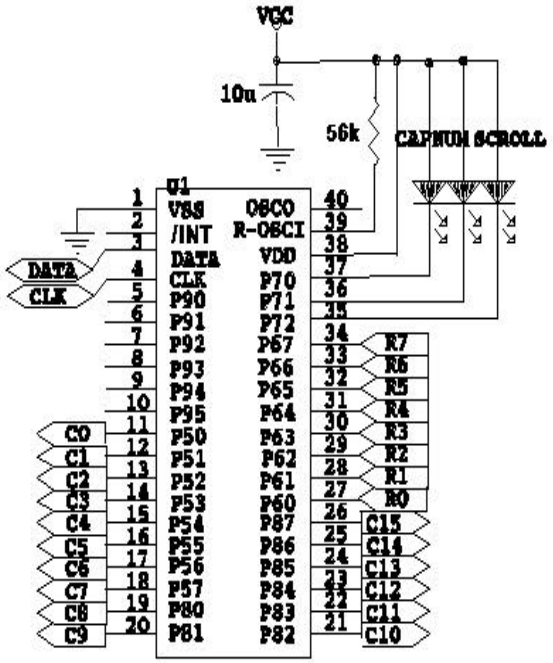
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle		45	50	55	%
Tins	Instruction cycle time (CK2="0")	RC Type	500		DC	ns
Ttcc	TCC input period		(Tins+20)/N*			ns
Twdt	Watchdog timer period	Ta=25°C		18		ms
Tdrh	Device reset hold period	Ta=25°C		18[1]		ms

N= selected prescaler ratio.

[1] NOTE: Vdd = 5V, set up time period = 16.2ms ± 5%

Vdd = 3V, set up time period = 18.0ms ± 5%

7. APPLICATION CIRCUIT



EM78451

	R0	R1	R2	R3	R4	R5	R6	R7
C0			058				064	
C1		044					057	
C2	110	016	001	002	017	031	046	
C3	045	030	112	003	018	032	047	
C4	115	114	113	004	019	033	048	
C5	035	021	006	005	020	034	049	050
C6	036	022	007	008	023	037	052	051
C7		118	119	010	025	039	054	
C8	116	015	120	121		029	043	061
C9	117	028	013	009	024	038	053	
C10	041	027	012	011	026	040	042	055
C11		092	076	122	091	093	090	084
C12	099	097	075	123	096	098	095	089
C13	104	102	085	086	101	103	100	105
C14	083		080	081	106	108	126	079
C15	060			124	125			062

APPENDIX

Package Types:

OTP MCU	Package Type	Pin Count	Package Size
EM78451AP	DIP	40	600 mil
EM78451AQ	QFP	44	